Resilience-Assured Protective Control of DC/AC Inverters Under Unbalanced and Fault Scenarios

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***Abstract*—This paper presents a model predictive control (MPC)-based scheme in power distribution systems focused on protective control of distributed energy resources (DER) assuring performance resiliency under faults and unbalanced conditions. This scheme is applied to a three-phase four-leg voltage inverter which is able to effectively respond to unbalanced loads at the edge connection of the power electronics to the distribution grids. 3-D space vector modulation is utilized for synchronization and load control, enabled through a minimized weighted cost function. To achieve a smooth-enough recovery and resilient waveform response in the face of the grid prevailing conditions, a passive predictive sub-space modulation is enforced. In order to demonstrate the effectiveness of the proposed platform, a modified IEEE 13-bus feeder is utilized as a test case. Numerical investigations on different fault scenarios validate the effectiveness of the proposed protective control scheme helping secure the voltage source inverters against overloads.**

Keywords—Distributed energy resource (DER); voltage source inverter; model predictive control (MPC); protection and control; space vector modulation (SVM).

I. INTRODUCTION

WITH the growing paradigm of the worldwide energy consumption in the 21st century, environmental concerns and global warmings as well as fossil fuel shortages, renewables, and clean energy resources have been ubiquitously installed and operated in modern power systems. This observation has been trending higher in recent years in the US and around the world. The high proliferation of distributed energy resources (DER), enabled through the deployment and integration of low-cost solar power, wind turbines, and geothermal has, in one hand, resolved many load-balance challenges in transmission and distribution grids, while on the other, has introduced critical concerns on power grid operation, protection, and control due to their stochastic variability and intermittency over time.

While the cost of the solar panels and the corresponding devices follows a descending trend in recent years, damage of the solar PV array and DC-link converters can still be costly, negatively impacting the economic viability and attractiveness of DERs in real-world applications [1], [2]. Such damages can originate from the device aging and degradation, dirt and dust, as well as some prevailing conditions in the grid they are connected to, among many others. For instance, short circuits inside/outside the PV sources, or overloads at the grid-connected side of the DERs, can cause an overcurrent in the PV source and DC storage, consequently leading to lots of heat that will be generated in the PV panels. This may potentially impose a risk of fire for DERs even if such situations last only for a short period of time. An effective protection and control scheme centered on power electronic devices at the edge connection of DERs to the distribution grid is critical in order to prevent the disastrous consequences of the failure and ensured resilience.

Several research efforts have been reported in the literature on the protection concerns of the DERs and different protection schemes have been proposed to address the critical challenges of their integration in the grid [3]-[7]. Emilio proposed an adaptive overcurrent protection scheme in [3], where a fuse relay is suggested requiring a preset range of current for the relay breaker to get activated. During high impedance faults, the overcurrent is close to, but below, the preset minimum fault current and the relay may fail to trip as expected. In the worst case scenario when such faults happen adjacent to the DER unit, the absence of an effective and functionally-adaptive protection scheme with the requisite protective devices will cause the power source to be overloaded. In [4], a multi-frame digital protection scheme for DERs is proposed which relies on data collections from multiple protective devices across the grid. While effective in many scenarios, the functionality of this protection scheme extensively relies on inter-connecting and communication devices system-wide, resulting in a dependable and secure but costly solution. Moreover, failure (and delays) or malfunctioning of the communication devices will impede successful operation of the scheme. In [5], a multi-stage intelligent protective function is proposed which (i) measures the required data at the DER connection bus to detect the fault and (ii) monitors the transient energy, overcurrent, synchronizing state, DER current and load impedance at the connection bus. While a reliable communication from the central controller is needed to ensure an acceptable performance, losing data connection with the central controller will not sabotage the protection scheme, enabling it to function as a stand-alone device. One disadvantage of this intelligent relay is that it cannot afford to lose any measured data unless well programmed and any malfunction of the redundant stage would lead to relay miss-operations and unnecessary tripping.

Extensive fault analyses on the behaviors of inverter-interfaced DERs in response to different control schemes are conducted and reported in [6], where the experiment results show that a current-controlled inverter typically has the ability to resist the fault currents at a certain extent even under protection failure; however, results from [7] indicate that the current-controlled inverters will still get overloaded during ground fault overvoltage conditions. There are multiple reasons contributing to the overvoltage conditions in power systems: Lightning strikes, electromagnetically induced voltages, arc grounding, switching surges, and insulation failures can be highlighted among many others. In most cases, protection devices can arrest the overvoltage surges and protective relays can isolate the

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electrical components from long-term exposure to overvoltage conditions. However, protection failure does happen in practice, and deficiencies mentioned in the above schemes can also lead to protection malfunction. In particular, program logical control devices are widely utilized in today's protective relays and circuit breakers helping the system to undergo less severe conditions even during faults or overvoltage scenarios. Note that while the system can still continue operation under such prevailing conditions, the electrical power components will be stressed and their performance will be negatively affected over time. A proper control scheme which can tolerate protection failure is hence necessary to best protect the DERs in distribution systems.

An improved model predictive control (MPC)-based protective control algorithm is proposed in this paper, which primarily focuses on protecting the DERs and DC voltage sources in the grid from overloading conditions during faults. The entire effort is to ensure that the voltage source inverters are able to function properly (overload-free) and resiliently during faults. This paper is structured as follows: the basic concept of the current control and four-leg inverter switching technique are introduced in Section II. The proposed MPC algorithm and protective subspace modulation are presented next in Section III. To verify the promising performance of the proposed protection and control scheme, PSCAD simulations and numerical results are discussed in Section IV. And finally come the concluding remarks in Section V.

II. Basic Concepts & Background

A. Current Control Model for LC Branch

The generalized current control model for a voltage source inverter with an LC filter is demonstrated in Fig. 1 and can be described through the following equations:

$$V_i(t) = V_o(t) + L\frac{dI(t)}{dt} \tag{1}$$

$$V_o(t) = R\big(I(t) - I_c(t)\big) + L_o\left(\frac{dI(t)}{dt} - \frac{dI_c(t)}{dt}\right) \tag{2}$$

$$I_c(t) = C\frac{dV_o(t)}{dt} \tag{3}$$

$$R = real(Z)\ \ L = imag(Z)/(2\pi f) \tag{4}$$

where, R and L_o are the load resistance and inductive reactance, respectively. Employing the approximated derivatives, we will then have:

$$\frac{dy}{dt} \approx \frac{y[n] - y[n-1]}{T_s} \tag{5}$$

$$\frac{d^2y}{dt^2} \approx \frac{y[n] - 2y[n-1] + y[n-2]}{T_s^2} \tag{6}$$

Combining equations (1), (2) and (3), the inverter output current $I[n]$ can be estimated in (7). In the steady state scenarios, a future state of $I[n]$ can be estimated in (8) where n=n+1, C is much smaller than L_o and the sampling interval T_s is very small.

B. Four-Leg Inverter and the Space Vector Control Strategy

A four-leg inverter model can be realized by including another pair of switching gates to a three-leg inverter. The neutral branch is characterized via an inductor L_n to reduce the switch ripples and is connected to the common point of a three-phase LC filter to smoothen the unbalanced output. The configuration of a four-leg inverter focused in this paper is illustrated in Fig. 2.

Contrary to the case of a three-leg inverter where 3-D space vector modulation is considered via the Clarke transformation followed by the use of a stationary αβ-frame to form a 2-D plane, in case of a four-leg inverter, γ-sequence caused by the unbalances is added to form a stationary αβγ-frame modulation in a 3-D coordinate. The Clarke transformation matrix can then be presented as in (9),

$$C_{\alpha\beta\gamma} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{9}$$

The gate switch control combinations **G** are defined in (10)-(11).

$$\begin{aligned} \mathbf{G}_{\mathbf{upper}} &= [g_1 \quad g_3 \quad g_5 \quad g_7] \\ \mathbf{G}_{\mathbf{lower}} &= [g_2 \quad g_4 \quad g_6 \quad g_8] \end{aligned} \tag{10}$$

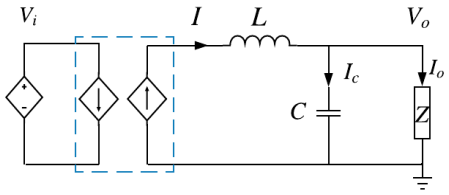


Figure 1. Branch diagram of a voltage source inverter with an LC filter.

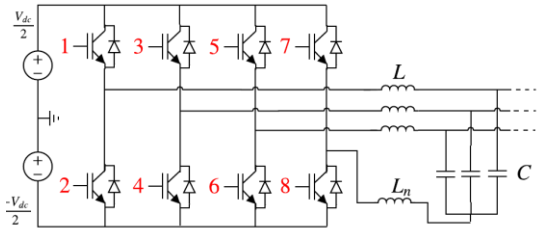


Figure 2. Diagram of a four-leg inverter with an LC filter.

$$I[n] = \frac{1}{RT_s + (L_o + L)}\left(T_sV_i[n] + (L_o + L)I[n-1] + \frac{(RCT_s + L_oC^2)V_o[n] - (RCT_s + 2L_oC^2)V_o[n-1]}{T_s} + \frac{L_oC^2V_o[n-2]}{T_s}\right) \tag{7}$$

$$I[n+1] = \frac{1}{RT_s + (L_o + L)}\left(T_sV_i[n+1] + (L_o + L)I[n] - \frac{(L_oC^2)(V_o[n] - V_o[n-1])}{T_s}\right) \tag{8}$$

$$\mathbf{G}_{\text{lower}} = 1 - \mathbf{G}_{\text{upper}} \tag{11}$$

The desired output current $I[n+1]$ in the next time-interval can be achieved by minimizing the weighted cost function **J** in (12) through substituting the $V_i[n+1]$ by different voltage values presented in Table I. The $V_i[n+1]$ which minimizes **J** is the predicted voltage of the inverter during the next iteration.

$$\mathbf{J} = W_1\left|I_\alpha - I_{a\_ref}\right| + W_2\left|I_\beta - I_{\beta\_ref}\right| + W_3\left|I_\gamma - I_{\gamma\_ref}\right| \tag{12}$$

III. The Proposed MPC-Based Control Scheme

In the proposed model predictive control (MPC) solution, we consider two different modes: PV control in normal operating states and the current control in abnormal operating states including faults and overvoltage conditions.

A. PV Output Power Control during Normal Operation

The PV power control diagram during normal operations is illustrated in Fig. 3. The power output from the PV array is estimated through the maximum power point tracking (MPPT). The error between the DC link and the optimal PV voltage is fed to a PI controller for maximum energy conversion. To achieve a desired current output during the MPC iterations, the transition from the present to the predicted switching pattern is modeled through a subspace vector as demonstrated in Fig. 4. To obtain an equivalently lower output voltage other than those listed in Table I, the switching intervals are distributed among three patterns: present, future, and null (zero voltage) according to the equivalent voltage magnitude and phase in $\alpha\beta\gamma$ – frame.

TABLE I
INVERTER OUTPUT VOLTAGE WITH THE GATE SWITCHING COMBINATION IN $\alpha\beta\gamma$- FRAME

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
$\mathbf{G_u}$	0000	0001	0010	0011	0100	0101	0110	0111
$\mathbf{V_\alpha}$	0	0	$-V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$	$-V_{dc}/3$	$-2V_{dc}/3$	$-2V_{dc}/3$
$\mathbf{V_\beta}$	0	0	$-V_{dc}/\sqrt{3}$	$-V_{dc}/\sqrt{3}$	$V_{dc}/\sqrt{3}$	$V_{dc}/\sqrt{3}$	0	0
$\mathbf{V_\gamma}$	0	$-V_{dc}$	$V_{dc}/3$	$-2V_{dc}/3$	$V_{dc}/3$	$-2V_{dc}/3$	$2V_{dc}/3$	$-V_{dc}/3$
	8	**9**	**10**	**11**	**12**	**13**	**14**	**15**
$\mathbf{G_u}$	1000	1001	1010	1011	1100	1101	1110	1111
$\mathbf{V_\alpha}$	$2V_{dc}/3$	$2V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/3$	0	0
$\mathbf{V_\beta}$	0	0	$-V_{dc}/\sqrt{3}$	$-V_{dc}/\sqrt{3}$	$V_{dc}/\sqrt{3}$	$V_{dc}/\sqrt{3}$	0	0
$\mathbf{V_\gamma}$	$V_{dc}/3$	$-2V_{dc}/3$	$2V_{dc}/3$	$-V_{dc}/3$	$2V_{dc}/3$	$-V_{dc}/3$	V_{dc}	0

$\mathbf{G_u}$: $\mathbf{G_{upper}}$

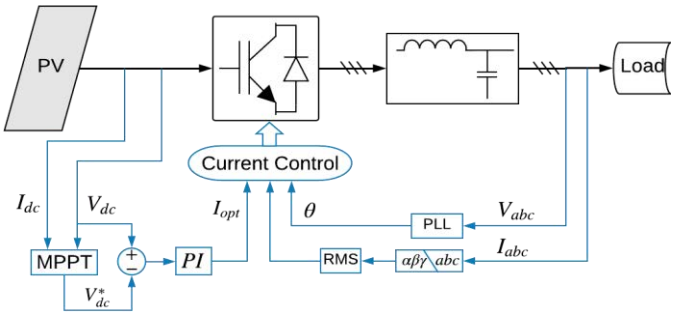


Figure 3. PV control diagram during nornal operating conditions.

B. Current Control during Fault and Overvoltage Scenarios

When a single line to ground (SLG) or double line to ground (LLG) faults happen, the phase voltage will decrease. The developed current control strategy helps the DC link not to get overloaded. In the face of overvoltage situations, each phase angle from the present switching pattern in 2-D ABC – frame can be obtained by (13).

$$\theta_{ph} = \frac{V_{ph,pre} \bullet V_{ph,fut}}{\left\|V_{ph,pre}\right\|\left\|V_{ph,fut}\right\|} \tag{13}$$

The modulation interval consisted of several MPC iterations is NT_s which is defined as

$$NT_s = T_0 + T_{pre} + T_{fut} + T_{15} \tag{14}$$

Where, T_{pre} and T_{fut} are the modulation intervals for the present and future patterns, respectively. Converting the voltage from ABC to $\alpha\beta\gamma$ – frame for the final modulation, we will have

$$T_{pre} \approx \frac{2}{\sqrt{3}} mNT_s \sin(\frac{\pi}{3} - \theta) \tag{15}$$

$$T_{fut} \approx \frac{2}{\sqrt{3}} mNT_s \sin(\theta) \tag{16}$$

$$m = \frac{2P}{V_{dc} I_{ref}} \tag{17}$$

$$\begin{bmatrix} V_\alpha[n+1] \\ V_\beta[n+1] \\ V_\gamma[n+1] \end{bmatrix} = C_{\alpha\beta\gamma} \begin{bmatrix} V_{A,fut} \\ V_{B,fut} \\ V_{C,fut} \end{bmatrix}, \quad \begin{bmatrix} V_\alpha[n] \\ V_\beta[n] \\ V_\gamma[n] \end{bmatrix} = C_{\alpha\beta\gamma} \begin{bmatrix} V_{A,pre} \\ V_{B,pre} \\ V_{C,pre} \end{bmatrix} \tag{18}$$

The overvoltage condition in the load will lead to a voltage increase in DC link, while a decrease can be seen in the value of m in (17). This, in return, reduces the activation time of the switching gate in every modulation interval and leads to more frequent zero-voltage outputs in the MPC iterations. Thus, a resilient protective control is achieved with the overvoltage condition being mitigated, the m value increased back to its standard, and the inverter is operating in a normal condition. Note that the future switching pattern is not unique when in a 3-D $\alpha\beta\gamma$ – frame; thus a passive predictive module is needed to record the future pattern and keep it updated in each full period.

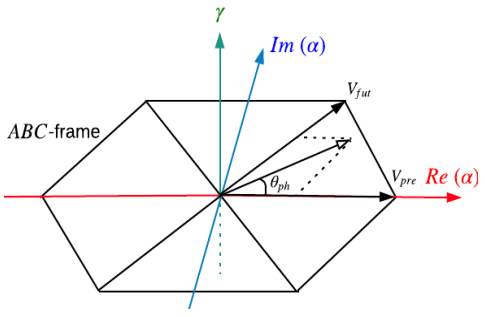


Figure 4. Subspace vector for current control during low power output and abnormal conditions.

IV. Simulation Results and Analysis

A grid-connected voltage source inverter has been modeled in PSCAD environment on an IEEE 13-Bus test feeder, the configuration of which is presented in Fig. 5.

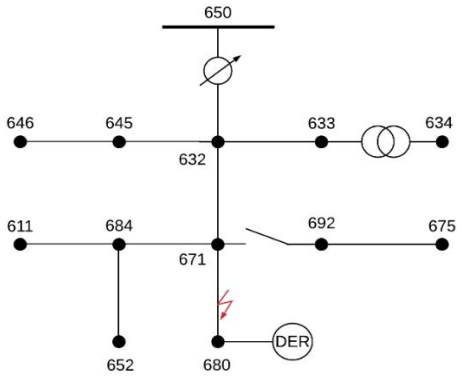


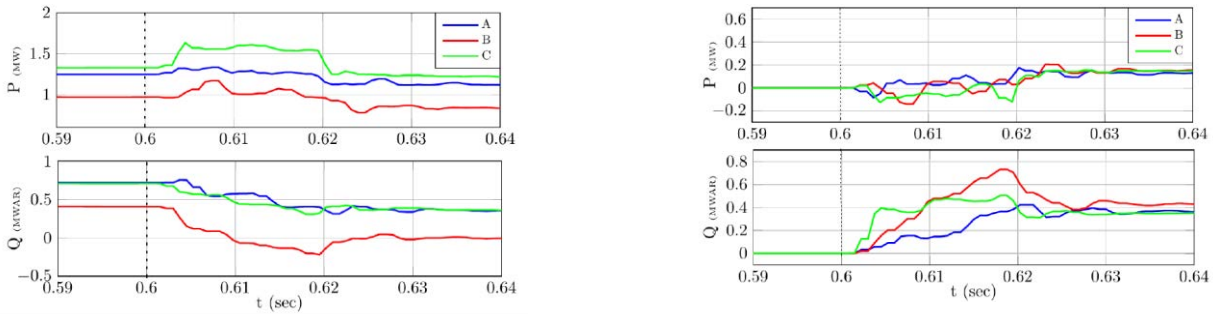
Figure 5. Configuration of the test system.

In order to verify the resilient performance of the suggested control scheme for the inverter during faults and breaker failure scenarios, all the breakers in the system are pre-set to be in their closed status and are supposed to fail to function during faults. The DER is assumed to be installed at Bus 680, and the fault location (on the feeder connecting bus 671 to 680) is illustrated in Fig. 5. The following test cases are studied:

1. Synchronized/connected renewable-based DER unit with a voltage source inverter to distribution system.
2. Single Line to Ground (SLG) fault on the feeder Phase A between Bus 671 and 680.
3. Line to Line (LL) fault on the feeder Phases A and B, between Bus 671 and 680.
4. Line to Line to Ground (LLG) fault on the feeder Phases A and B, between Bus 671 and 680.
5. Simulated overvoltage condition added to Phase A.

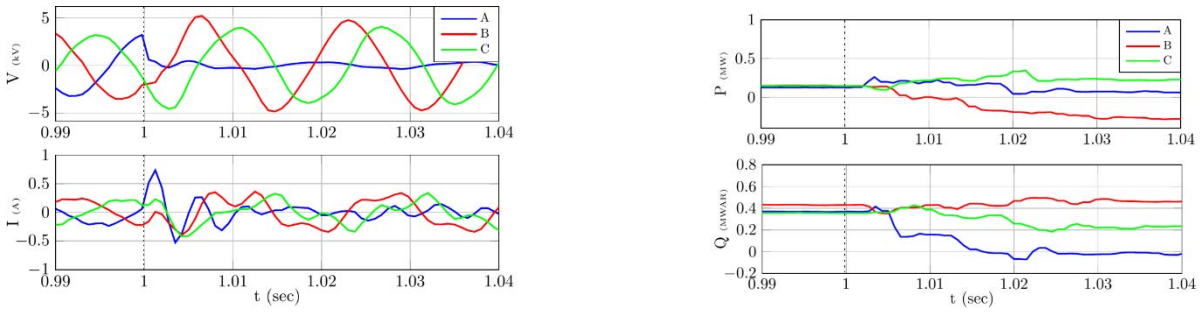
As demonstrated in Fig. 6, the DER is functional, synchronized, and delivers power when connected to the grid (test case 1). In the case of an SLG fault (test case 2), the voltage in Phase A drops to almost zero as shown in Fig. 7 (a), and an overvoltage occurred at Phases B and C accordingly. The real power output in Phase C slightly increased. At the same time, the real power output in Phase B appears negative and the reactive power in phases A and C decrease. The total real and reactive power output of the DER, however, decreased overally, which represents a safe and overload-free operation, and verifies the advantage of the proposed control scheme.

During the LL fault (test case 3), no variation is observed in the power output in Phase C, while both real and reactive power output have decreased in Phase A and Phase B (see Fig. 8). Therefore, the performance of the proposed scheme is validated in this case as well. When the system suffers an LLG fault between Bus 671 and 680 (test case 4), the DER behavior is observed similar to that during the LL fault (test case 3). However, the real power output in Phase C has dropped (see Fig. 9). Meanwhile, the reactive power in Phase C varies at the moment when the LLG fault happens and it gradually decreased as the system approaches a steady state condition. When the LLG fault is cleared, the power output recovers to a normal state within 0.05 sec., and a resilient performance is achieved.



(a) (b)

Figure 6. Three-phase power when the DER is plugged-in: (a) power injection from Bus 650; (b) power injection from the DER unit.



(a) (b)

Figure 7. Single Line to Ground (SLG) fault at Phase A: (a) three phase voltage at Bus 671; (b) power injection from the DER unit.

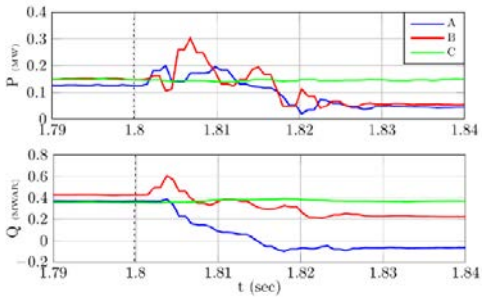


Figure 8. Line to Line (LL) fault at Phases A and B: three-phase power output from the DER unit.

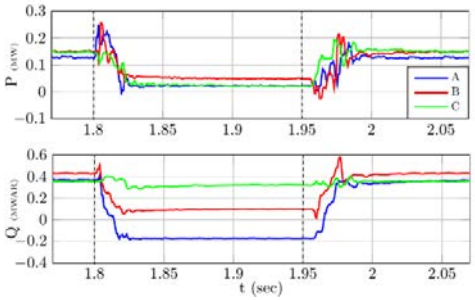
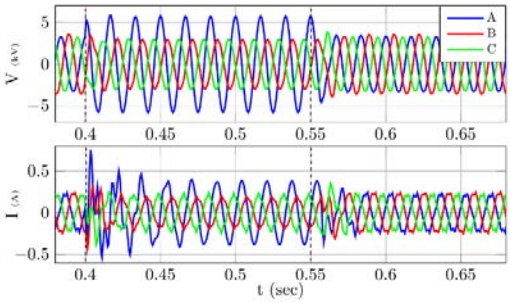
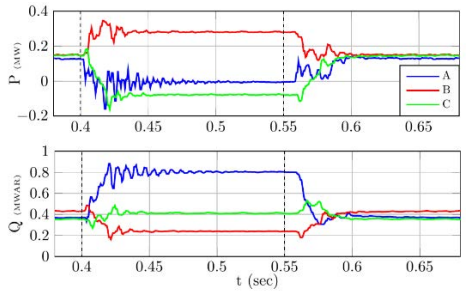


Figure 9. Line to Line to Ground (LLG) fault at Phases A and B: three-phase power output from the DER unit.



(a)



(b)

Figure 10. Single-phase overvoltage at Phase A: (a) three-phase voltage at Bus 671; (b) three-phase power output from the DER unit.

To further validate the proposed protective control scheme, an artificial overvoltage is simulated and added to Phase A. According to the simulation results in Fig. 10, the real power at Phases A drops to zero, still with some distortions observed at Phase A. At the same time, an increase in the real power output at Phase B can be observed; with the negative power output at Phase C, the overall real power output decreases. The reactive power at Phase A significantly increased, while the power from the DC link has decreased (see Fig. 11), which reflects that the power filter is consuming more reactive power during the overvoltage condition. So, the proposed control scheme is proven resilience-effective under overvoltage scenarios, with a recovery time of 3 periods, and the DC source will not damage.

V. Conclusion

In this paper, an MPC-based protective control scheme is proposed for voltage source inverters at the edge connection of DER units to power distribution systems. The developed scheme ensures a protective control of such power electronic devices under faults and overloading scenarios—when protective devices may fail to operate—and allows a resilient operation of the DER units following the fault clearance.

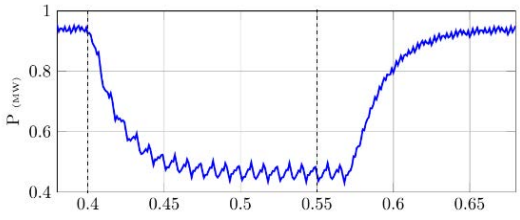


Figure 11. DC link output power during an arterial overvoltage.

Simulations on the IEEE 13-bus test feeder with multiple test cases revealed that the proposed scheme is able to secure an acceptable performance of the voltage source inverter under fault and unbalanced conditions, potentially immunizing the DC source from damage even without a proper operation of the network protective devices. Future research may be focused on the design of the effective power filters during such prevailing conditions as their damage is an impediment to a successful operation of the DER units even when the faults are cleared.

References

[1] Z. Yi and A. H. Etemadi, "Fault Detection for Photovoltaic Systems Based on Multi-Resolution Signal Decomposition and Fuzzy Inference Systems," *IEEE Trans. on Smart Grid*, vol. 8, no. 3, pp. 1274-1283, 2017.

[2] Z. Yi and A. H. Etemadi, "Line-to-Line Fault Detection for Photovoltaic Arrays Based on Multiresolution Signal Decomposition and Two-Stage Support Vector Machine," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8546-8556, Nov. 2017.

[3] E. C. Piesciorovsky and N. N. Schulz, "Fuse relay adaptive overcurrent protection scheme for microgrid with distributed generators," *IET Gen., Trans. & Dist.*, vol. 11, no. 2, pp. 540-549, 2017.

[4] S. A. Saleh, R. Meng, R. McSheffery, S. E. Buck and E. Ozkop, "Performance of Multiframe Digital Interconnection Protection for Distributed Cogeneration Systems," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1166-1181, March-April 2018.

[5] K. Lai, M. S. Illindala and M. A. Haj-ahmed, "Comprehensive Protection Strategy for an Islanded Microgrid Using Intelligent Relays," *IEEE Trans. on Industry Applications*, vol. 53, no. 1, pp. 47-55, Jan.-Feb. 2017.

[6] Z. Shuai, C. Shen, X. Yin, X. Liu and Z. J. Shen, "Fault Analysis of Inverter-Interfaced Distributed Generators With Different Control Schemes," *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1223-1235, June 2018.

[7] M. Ropp, *et al.*, "Ground Fault Overvoltage With Inverter-Interfaced Distributed Energy Resources," *IEEE Transactions on Power Delivery,* vol. 32, no. 2, pp. 890-899, April 2017.